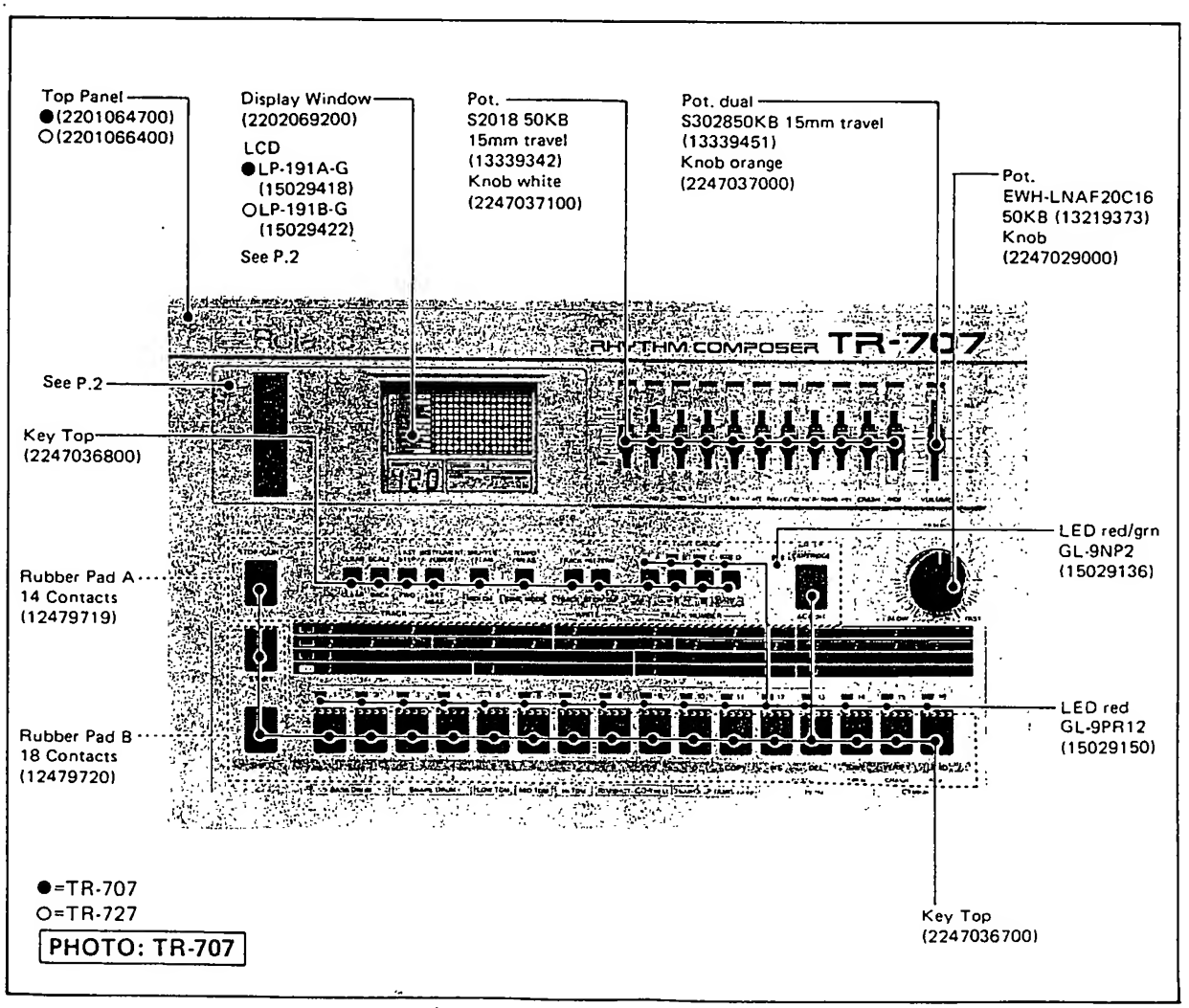
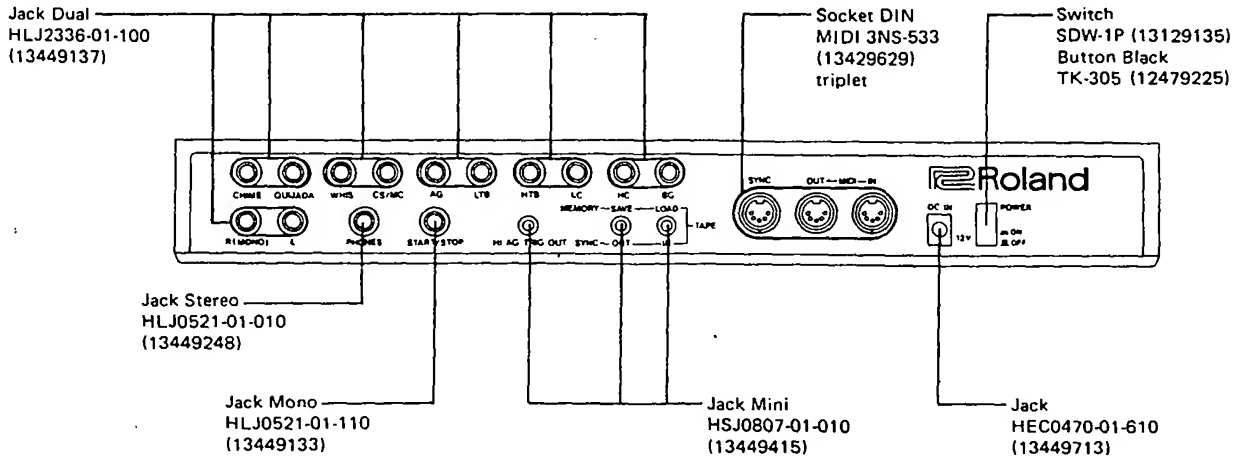
# TR-707/727 SERVICE NOTES

*First Edition*

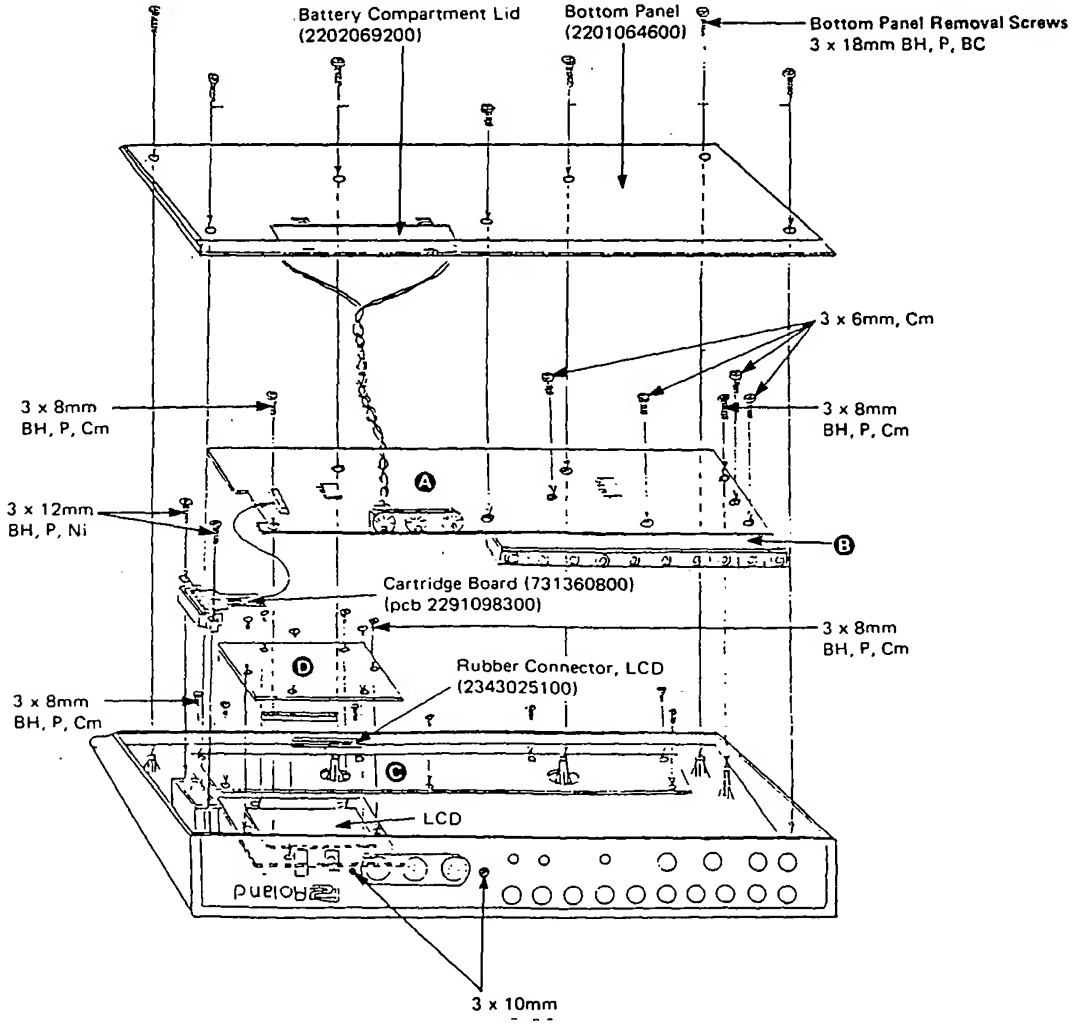
## SPECIFICATIONS

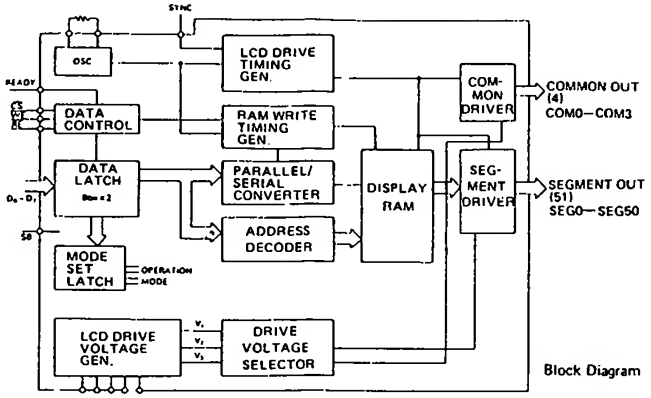
| | | |
|---|---|---|
| Memory Capacity | : | 64 Rhythm Patterns (16 x 4 Group) |
| Track | : | 4 (1 to 4; continuous Maximum measures=998) |
| Step | : | 1 to 16 steps/measure |
| Tempo | : | ♩ = 38 to 250 |
| Rear Panel | : | Master Out (L,R/MONO) [8Vp-p, 1KΩ] |
| Trigger Out | : | +5V, 20ms Pulse TR-707 . . . . . Rim Shot<br>TR-727 . . . . . Hi Agogo |
| Sync In/Out (5P DIN) | : | (1: Run/Stop, 2: GND, 3: Clock, 4: NC, 5: Continue) |
| Power Consumption | : | 2.4 W |
| Dimensions | : | 380 (W) x 73 (H) x 250 (D) mm<br>14-15/16" (W) x 2-7/8" (H) x 9-13/16" (D) in |
| Weight | : | 1.5 kg/13 lb. 5 oz. |
| Accessories | : | 12V AC Adaptor<br>Connection Cord PJ-1 |
| Options | : | Memory Cartridge M-64C<br>Pedal Switch DP-2 |






| | TR-707 | TR-727 |
|---|---|---|
| Ⓐ | Voicing Board (7313604000) (pcb 2291098102) | Voicing Board (7313804000) (pcb 2292018900) |
| Ⓑ | Volume Board (7313605000) (pcb 2291098002) | Volume Board (7313805000) (pcb 2292019000) |
| Ⓒ | Switch Board (7313606000) (pcb 2291097903) | |
| Ⓓ | LCD Board (7313607000) (pcb 2291098203) | |

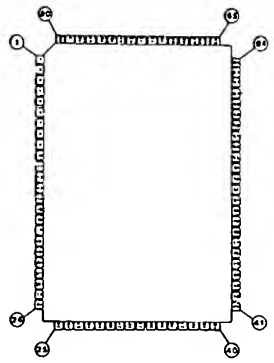





Block Diagram

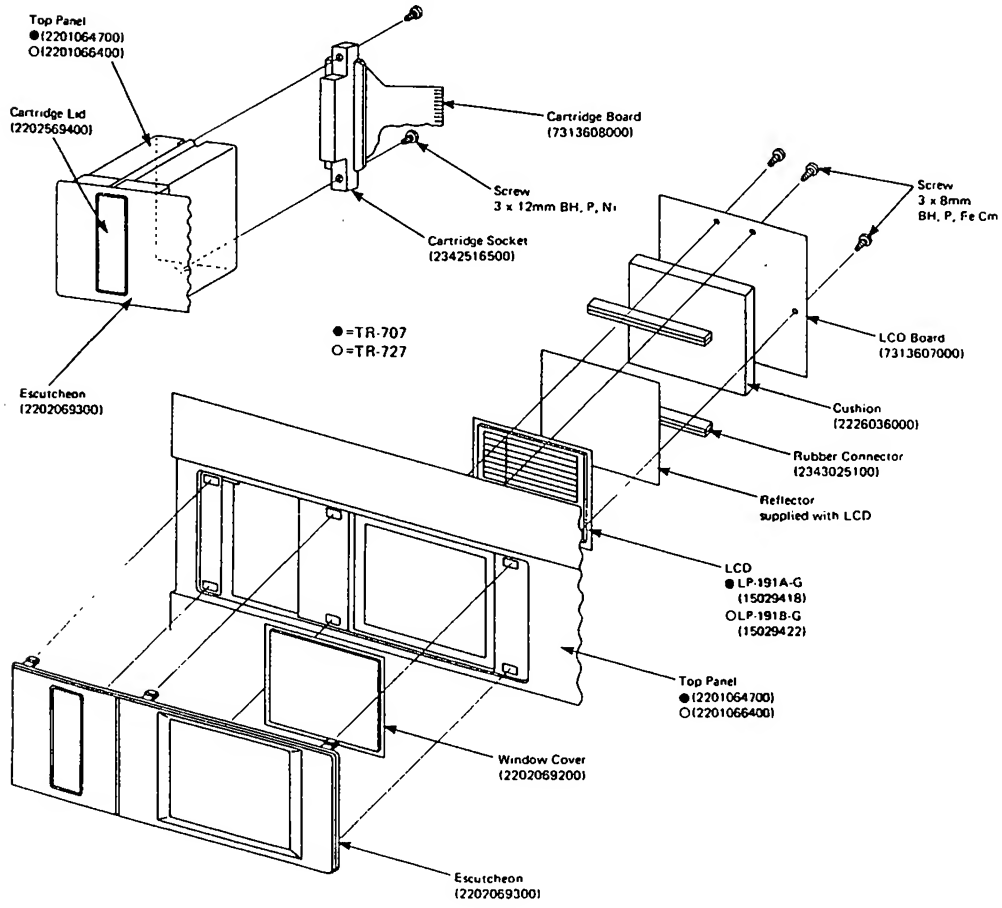
## LCD Driver
HD61602

Pin configuration
(Top View)



TERMINAL ASSIGNMENTS

| Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|---|---|
| 1 | Vdd | 28 | SEG49 | 55 | SEG22 |
| 2 | READY | 29 | SEG48 | 56 | SEG21 |
| 3 | CS | 30 | SEG47 | 57 | SEG20 |
| 4 | WE | 31 | SEG46 | 58 | SEG19 |
| 5 | RE | 32 | SEG45 | 59 | SEG18 |
| 6 | SD | 33 | SEG44 | 60 | SEG17 |
| 7 | D7 | 34 | SEG43 | 61 | SEG16 |
| 8 | D6 | 35 | SEG42 | 62 | SEG15 |
| 9 | D5 | 36 | SEG41 | 63 | SEG14 |
| 10 | D4 | 37 | SEG40 | 64 | SEG13 |
| 11 | Vss | 38 | SEG39 | 65 | SEG12 |
| 12 | D3 | 39 | SEG38 | 66 | SEG11 |
| 13 | D2 | 40 | SEG37 | 67 | SEG10 |
| 14 | D1 | 41 | SEG36 | 68 | SEG9 |
| 15 | D0 | 42 | SEG35 | 69 | SEG8 |
| 16 | Vref1 | 43 | SEG34 | 70 | SEG7 |
| 17 | Vref2 | 44 | SEG33 | 71 | SEG6 |
| 18 | VC2 | 45 | SEG32 | 72 | SEG5 |
| 19 | VC1 | 46 | SEG31 | 73 | SEG4 |
| 20 | V1 | 47 | SEG30 | 74 | SEG3 |
| 21 | V2 | 48 | SEG29 | 75 | SEG2 |
| 22 | V3 | 49 | SEG28 | 76 | SEG1 |
| 23 | COM0 | 50 | SEG27 | 77 | SEG0 |
| 24 | COM1 | 51 | SEG26 | 78 | SYNC |
| 25 | COM2 | 52 | SEG25 | 79 | OSC2 |
| 26 | COM3 | 53 | SEG24 | 80 | OSC1 |
| 27 | SEG50 | 54 | SEG23 | — | — |




# PARTS LIST
## EXCLUSIVE PARTS

### TR-707

**CASING**

| | | |
|---|---|---|
| 2201064700 | Top Panel | |

**PCB**

| | | |
|---|---|---|
| 7313604000 | Voicing Board | (pcb 2291098102) |
| 7313605000 | Volume Board | (pcb 2291098002) |

**LCD**

| | | |
|---|---|---|
| 15029418 | LCD | LP-191A-G |

**IC**

Program ROM

| | | |
|---|---|---|
| 15179720 | HN4827128G-25 | NMOS EPROM<br>(Ver.0 SN460100-504399)<br>(Ver.1 SN504400-519599) |
| or | | |
| 15179660 | HN613128PE95 | CMOS MASK ROM<br>(Ver.1 SN519600-533099) |
| or | | |
| 15179692 | HN613128PG24 | CMOS MASK ROM<br>(Ver.2 SN533100-up) |

UPWARD COMPATIBILITY

Ver.0

In Pattern PLAY mode -- Selecting a pattern from different scale while repeating STOP and START or CONTINUE sometimes leads to Power-ON initialization.
ROMs of Ver. 1 always run the new pattern at the beginning of a measure.

Ver.1

When the unit is used as a Master -- Repetitions of STOP and CONTINUE more than 30 times would cause generation of a redundant MIDI clock $F8.
When the unit is used as a Slave -- Will miss a MIDI IN clock when STOP signal follows the Clock within 1ms.

MASK ROM of Ver.2 cures this problem.
For a replacement Ver.2 or up is recommendable.
上位コンパチなので補修用としてはバージョン番号の大きいPROMの使用が望ましい。

Sound ROM

| | | |
|---|---|---|
| 15179661 | HN61256PC-71 | CMOS MASK ROM<br>BD1/2, SD1/2, LT, MT |
| 15179662 | HN61256PC-72 | CMOS MASK ROM<br>HT, Open/Closed H.H, Rim, Cow<br>HCP, Tambourine |
| 15179663 | HN61256PC-73 | CMOS MASK ROM<br>Crash Cymbal |
| 15179664 | HN61256PC-74 | CMOS MASK ROM<br>Ride Cymbal |

### TR-727

**CASING**

| | | |
|---|---|---|
| 2201066400 | Top Panel | |

**PCB**

| | | |
|---|---|---|
| 7313804000 | Voicing Board | (pcb 2292018900) |
| 7313805000 | Volume Board | (pcb 2292019000) |

**LCD**

| | | |
|---|---|---|
| 15029422 | LCD | LP-191B-G |

**IC**

Program ROM

| | | |
|---|---|---|
| 15179719 | HN4827128G-25 | NMOS EPROM |

Sound ROM

| | | |
|---|---|---|
| 15179694 | HN61256PC-79 | CMOS mask ROM<br>HI/LOW BONGO, HI CONGA<br>LOW CONGA, HI TIMBALE |

| | | |
|---|---|---|
| 15179695 | HN61256PC-80 | CMOS mask ROM<br>LOW TIMBALE, AGOGO, CABASA<br>MARACAS, WHISTLE |
| 15179696 | HN61256PC-81 | CMOS mask ROM<br>QUIJADA |
| 15179697 | HN61256PC-82 | CMOS mask ROM<br>STAR CHIME |

## COMMON PARTS

### CASING

| | | |
|---|---|---|
| 2201064600 | Bottom Case | |
| 2202069100 | Battery Cover | |
| 2202069200 | Display Window | |
| 2202069300 | LCD Escutcheon | |
| 2202569400 | Cartridge Lid | |

### KNOB, BUTTON, KEY TOP

| | | | |
|---|---|---|---|
| 2247029000 | Knob | gray | TEMPO |
| 2247036700 | Key Top (large) | gray | Main Key 1-16,ENTER, START,SHIFT,STOP/CONT |
| 2247036800 | Key Top (small) | gray | |
| 2247037100 | Knob | white | BD,SD,LT,MT,HT,OCH, RS/CB,HCP/TAMB,RIDE, CRASH |
| 2247037000 | Knob | orange | VOLUME |
| 12479225 | TK-305 | black | POWER |

### PCB ASSY

| | | |
|---|---|---|
| 7313606000 | Switch Board | (pcb 2291097903) |
| 7313607000 | LCD Board | (pcb 2291098203) |
| 7313608000 | Cartridge Board | (pcb 2291098300) |

### COIL, TRANSFORMER

| | | | |
|---|---|---|---|
| 2244025000 | S097744 | Transformer | DC/DC convertor |
| 12449229 | FKOB160MH15 | Coil | line filter |

### SOCKET

| | | |
|---|---|---|
| 13429629 | MIDI 3-NS-533 | DIN |
| 13449713 | HEC0470-01-610 | AC adapter |
| 13449415 | HSJ0807-01-010 | mini |
| 13449248 | HLJ0521-01-010 | stereo |
| 13449133 | HLJ0521-01-110 | monoral |
| 13449137 | HLJ2336-01-100 | dual |
| 2342516500 | PBRS-28U-T01-S | cartridge |

### SWITCH

| | | |
|---|---|---|
| 12479719 | Rubber switch (Pad) A | 14 contact upper row |
| 12479720 | Rubber switch (Pad) B | 18 contact lower row |
| 13129135 | SDW-1P | POWER |

### POTENTIOMETER

| | | |
|---|---|---|
| 13339342 | S2018 50KB | slide 15mm travel |
| 13339451 | S3028 50KB | dual slide 15mm travel |
| 13219373 | EWH-LNAF20C16 50KB | TEMPO |
| 13299136 | RVF8P01-503 50KB | trimmer |
| 13299141 | RVF8P01-204 200KB | trimmer |

### XTAL, CERAMIC RESONATOR

| | | |
|---|---|---|
| 12389736 | HC-18/U | 4.0MHz Xtal |
| 12389735 | CSA 1.6MK | 1.6MHZ ceramic resonator |

### IC

| | | |
|---|---|---|
| 15229825 | RD63H114PF | gate arrey |
| 15179200 | HD6303XF | CPU |
| 15179340 | HM6116LP-4 | CMOS S RAM |
| 15219148 | HD61602 | LCD driver |
| 15159503 | TC40H000P<br>quad 2-input NAND gate | H CMOS |
| 15159504 | TC40H002P<br>quad 2-input NOR gate | H CMOS |
| 15159505 | TC40H004P<br>hex inverter | H CMOS |
| 15159517 | TC40H010P<br>triple 3-input NAND gate | H CMOS |
| 15159506 | TC40H138P<br>3-to-8 line decoder/demutltiplexer | H CMOS |
| 15159535 | TC40H151P<br>1-of-8 data selector/multiplexer | H CMOS |
| 15159511 | TC40H174P<br>hex D-type flip flop | H CMOS |
| 15159524 | TC40H245P<br>octal bidirectional bus buffer | H CMOS |
| 15159507 | TC40H273P<br>octal D-type flip flop | H CMOS |
| 15159530 | TC40H367P<br>hex bus buffer | H CMOS |
| 15159104 | TC4011BP<br>quad 2-input NAND gate | CMOS |
| 15159105 | TC4013BP<br>dual D-type flip flop | CMOS |
| 15159141 | HD14040BP<br>12-stage binary counter | CMOS |
| 15159113 | HD14051BP<br>single 8-channel multiplexer/demultiplexer | CMOS |
| 15159301 | TC4520BP<br>dual binary up counter | CMOS |
| 15159303 | HD4584BP<br>hex schmitt trigger | CMOS |
| 15189136 | M5218L | Op amp |
| 15189154 | TL064 | FET Op amp |
| 15219147 | UPC624C | D/A convertor |
| 15199108F0 | UA78M05UC | voltage regurator +5V |
| 15229712 | PC900 | photo coupler |
| 15149118 | M54517P | transistor array |

### TRANSISTOR

| | | |
|---|---|---|
| 15129612 | 2SD1469-R | NPN |
| 15129137 | 2SC2603-F | NPN |
| 15129412 | 2SC1384-Q | NPN |
| 15119125 | 2SA1115-F | PNP |
| 15139101 | 2SK30ATM-Y | FET |

### DIODE

| | | |
|---|---|---|
| 15019126 | 1SS113T-77 | diode |
| 15019209T0 | S-5500G | rectifier |
| 15019667 | RD-12EB1-T | 12V zener |
| 15029136 | GL-9NP2 | LED red/grn |
| 15029150 | GL-9PR12 | LED red |

### RESISTOR ARRAY

| | | |
|---|---|---|
| 13919133 | RKM7LM502 | D/A converter |
| 13919103 | RGSD8X103J | 10K x 8 |
| 13919113 | RGSD4X103J | 10K x 4 |
| 13910107 | RSD8X332J | 3.3K x 8 |

### CONNECTOR

| | | |
|---|---|---|
| 13439256 | 5089-11A | 11P (Switch pcb) |
| 13439255 | 5089-13A | 13P (Switch pcb) |
| 13439253 | 5494-9C | 9P (Voicing pcb) |
| 13439252 | 5494-10C | 10P (Voicing pcb) |
| 13439254 | 5597-28APB | 28P (Voicing pcb) cartridge |
| 2343025100 | | rubber connector LCD |

### WIRING ASS'Y

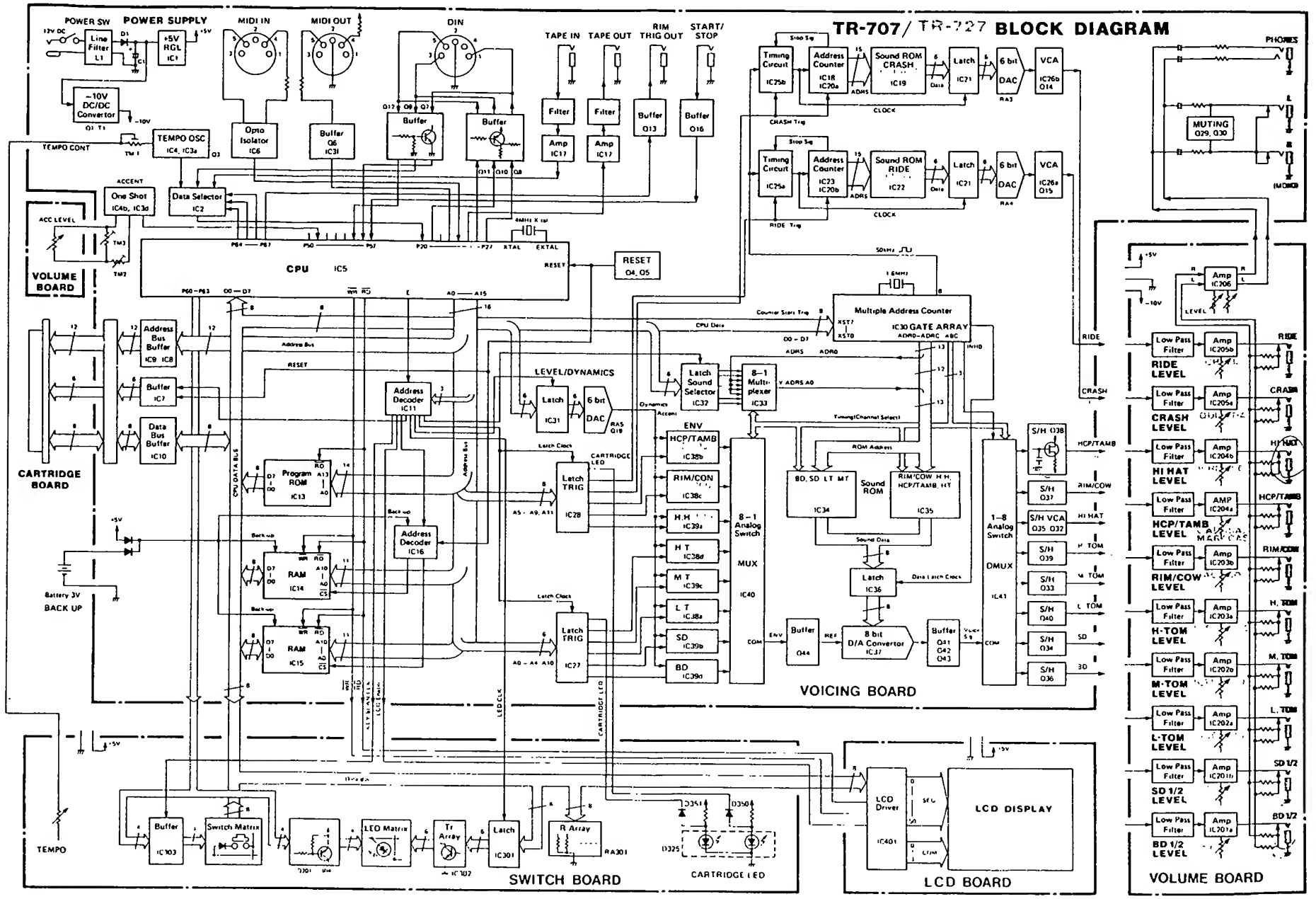
| | | |
|---|---|---|
| 2341048000 | 13P | (LCD pcb) |
| 2341047900 | 11P | (Voicing pcb) |
| 2347015200 | 9P flat cable | (Volume pcb) |
| 2347015300 | 10P flat cable | (Volume pcb) |

### MISCELLANEOUS

| | | | |
|---|---|---|---|
| 2217515300 | Spring | | RAM cartridge |
| 2214531300 | Shaft | | RAM cartridge |
| 2345014600 | Plate | | battery |
| 12469117 | Heat Sink MT-25-BS | | |
| 2219049900 | LED Holder | | (switch pcb) |
| 13529117 | Ceramic Capacitor | D55Y5V1H334Z21<br>0.33μF | (LCD pcb) |
| 12559708 | Fusing Resistor | FRN8 1/4W2.7Ω | |
| 2225022801 | Shield Cover | | top panel |
| 2225022400 | Shield | | (Voicing pcb-Volume pcb) |

### COMMERCIALLY AVAILABLE ACCESSORIES

| | | |
|---|---|---|
| 12569105 | Dry cell SUM-3S 1.5V | |
| 12449538 | 12V AC adapter (100V) | |
| 12449539 | 12V AC adapter (117V) | |
| 12449540 | 12V AC adapter (220V) | |
| 12449541 | 12V AC adapter (240VA) | Australian |
| 2343067500 | Connection Cable LP-25 | |


TR-707/ TR-727 BLOCK DIAGRAM
POWER SW
POWER SUPPLY
MIDI IN
MIDI OUT
DIN
TAPE IN
TAPE OUT
RIM TRIG OUT
START/ STOP
PHONES
MUTING
CPU IC5
RESET
VOLUME BOARD
CARTRIDGE BOARD
Program ROM
RAM
Battery 3V BACK UP
Address Decoder
Data Selector
Address Bus Buffer
Data Bus Buffer
LEVEL/DYNAMICS
Latch Sound Selector
8-1 Multiplexer
Multiple Address Counter
IC30 GATE ARRAY
Sound ROM CRASH
Sound ROM RIDE
Timing Circuit
Address Counter
Latch
6 bit DAC
VCA
ENV
HCP/TAMB
RIM/CON
H.H
H T
M T
L T
SD
BD
8-1 Analog Switch
MUX
Sound ROM
BD, SD, LT, MT
RIM/COW, H.H, HCP/TAMB, HT
1-8 Analog Switch
DMUX
8 bit D/A Convertor
S/H
S/H VCA
Latch TRIG
Buffer
Amp
Low Pass Filter
RIDE LEVEL
CRASH LEVEL
HI HAT LEVEL
HCP/TAMB LEVEL
RIM/COW LEVEL
H-TOM LEVEL
M-TOM LEVEL
L-TOM LEVEL
SD 1/2 LEVEL
BD 1/2 LEVEL
VOICING BOARD
SWITCH BOARD
CARTRIDGE LED
LCD Driver
LCD DISPLAY
LCD BOARD
VOLUME BOARD
TEMPO
TEMPO OSC
One Shot
Opto Isolator
Filter
Amp
Buffer
Switch Matrix
LED Matrix
Tr Array
R Array

# CIRCUIT DESCRIPTIONS

TR-707 and TR-727 are designed based on the same circuit configuration, having more in common with each other. The differences between two models are sound data, component values in several audio stages and a couple of pin connections at IC30 of Voice board.

Both models derive all rhythm sounds from PCM-encoded samples of real sounds stored in ROM. Each waveform is stored either independently (e.g. CYMBAL) or together with another waveform as shown in Tables 1 and 2. Accordingly, sound reproducing circuits are classified into two: multiplex and single. The following description focuses on PCM sound reproduction system, taking TR-707 circuits as a representative.

# 回路解説

TR-707/727はROMにメモリされているPCM波形（サウンドデータ）を音源として利用しています。楽器の種類が異なる為一部に結線や定数の違いがあるものの、全体の回路構成は両機種に共通です。以下TR-707を例にとって説明します。

表1及び2から判る様に、IC34、IC35には複数音源のデータが、IC19、IC22には単一音源がメモリされています。従って、これら音源データの読み出しから再生までの過程もシングル方式とマルチの二種類があります。

## MULTIPLEX SOUND PROCESSING

### MULTIPLE ADDRESS COUNTERS

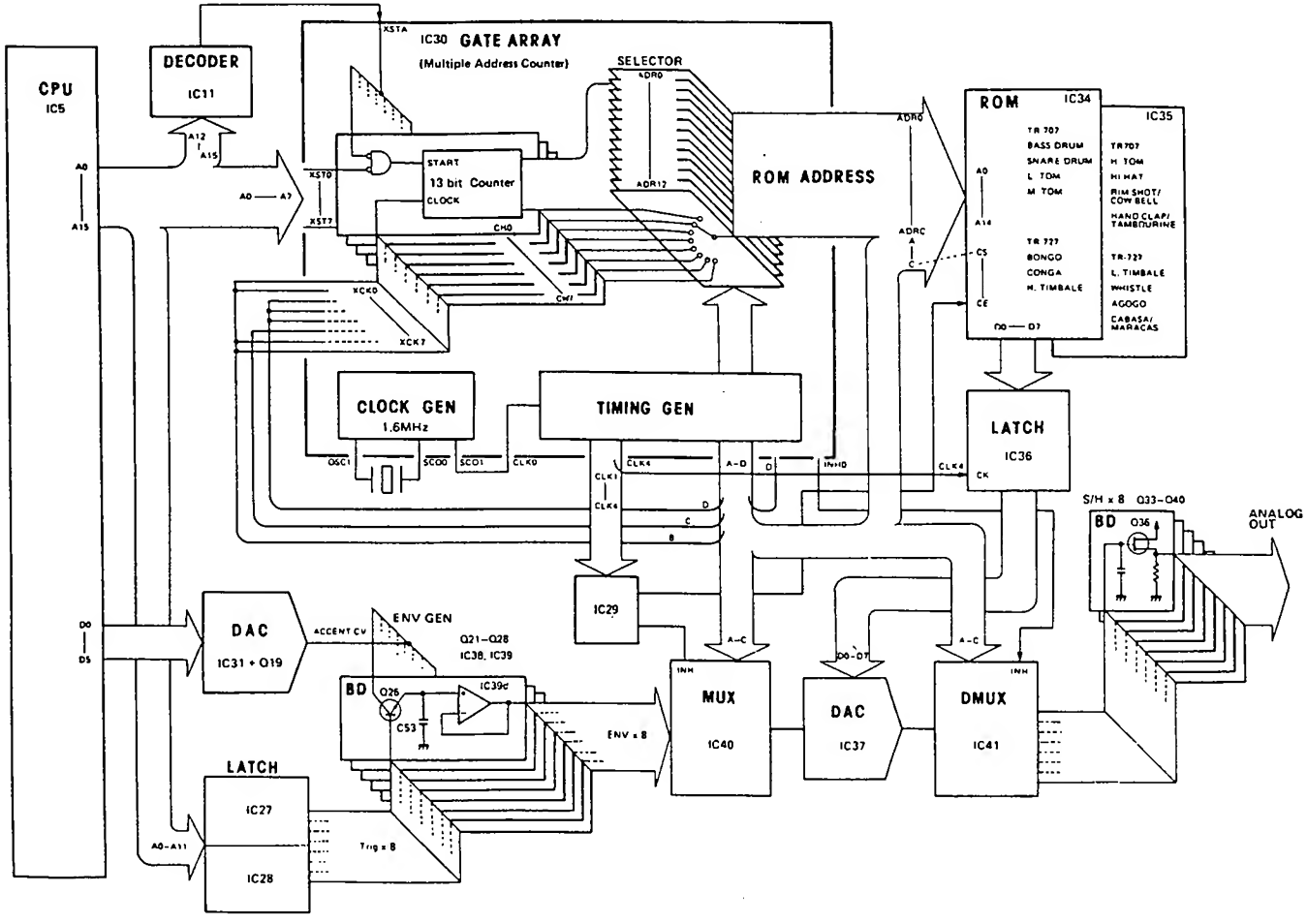
IC30 RD63H114 on Voicing Board is a custom-LSI(called Gate Array) designed for use in PCM-sound multi-rhythm systems. The LSI assumes the key role in the TR-707 sound system. It incorporates a master clock generator, timing generator and 8 13-bit address counters. The timing generator, not only supplies clocks to these counters for generating address bits, but also feeds peripheral circuits with various timing clocks to sync the entire system operation. Of these timing clocks, A, B and C together make a channel-select code for signaling the ROMs (ICs 34, 35), MUX IC40 and DMUX IC41 which voice is being addressed by an address counter in IC30.

## マルチ音源

### マルチプル・アドレスカウンタ

多音源データをメモリしているROM（IC34，35）からのデータ読み出し、D/A変換、S/Hおよびその他の関連回路は、IC30 RD63H114をマスターとして動作します。RD63H114はマルチ音源機器用に開発されたカスタムLSIであって、内蔵のクロックおよびタイミング発生回路によりこれら外付回路を同期させるクロック信号を出力します。同期クロックのうちA，B，Cはボイス・チャンネルのセレクトコードを形成しますので特に重要です。IC30はROM（IC34，35）内の各音源データのアドレスを次々と出力して行きますが、A，B，Cは今どの音源アドレス（アドレス・カウンタのチャンネル番号）が出力されているかを、ROM以外のMUX IC40，DMUX IC41にも知らせます。（例SDの場合 A＝1，B＝0，C＝0。次頁のタイミングチャート参照）

## MULTIPLEX SOUND SYSTEM BLOCK DIAGRAM



Now suppose that TR-707 is to run with BASS DRUM 1(BD-1) being selected, the CPU IC5 puts XST0 (CH0 start) and XSTA (XST0–XST7 enable) low, resetting counter 0, presetting it to the starting address 0000H and allowing it to count the clock pulse XCK0 from pin B in discrete steps. The counter continues counting until it increments up to 1FFFH and tops there until the next trigger pulse is received. While counting, the contents (a group of 13 clock pulses) of the counter is transferred to address selector where it is read every 40μs and is presented along ports ADR0 through ADRC––13 lower address bits.

## PCM MEMORY READING

IC34 and IC35, 32,768 word by 8 bit ROM, require 15 address bits to access their memory locations. Clocks A and B from IC30 serve as MSBs while C indicates which one of two ROMs is to be selected––Chip Select.

On the contrary, LSB ADR0 is defeated when particular voice is selected: BD-1 and BD-2 share the same memory area with even addresses allocated to BD-1 and odd ones to BD-2 as shown in Table 1. With BD-1, data selector IC33 blocks ADR0 and passes "0" data from IC32 onto A0 of ROM IC35. With BD-2, IC33 selects "1". With Low Tom, Mid Tom, Hi Tom or Hi Hat, ADR0 is allowed to reach A0.

Each 8-bit memory location (PCM waveform data) in ROM is loaded into latch IC36 on the rising edge of CLK4. This 8 bit data is, if converted to analog equivalent by D/A converter IC37 as it is, not restored to its original amplitude. A certain technic is involved during PCM to improve S/N ratio, to have higher resolution, etc. A signal coming from Envelope Generator into (+) REF pin gives right tone contour to a continual PCM waveforms being decoded and converted to an analog sound.

今 BASS DRUM1（BD−1）が選択された状態で、リズムが止ったとすると、IC30に$\overline{XST0}$（チャンネル0スタート）と$\overline{XSTA}$（XST0−7イネーブル）が加わり、カウンタCH0は0000Hにリセットされた後XCK0に加えられて来るクロックBをカウントして行きます。この13ビット・アドレスカウンタのカウント値は40μs毎にアドレス・セレクタによりADR0−ADRC端子に出力されて行きます。（次にもう一度$\overline{XST0}$が加わらない場合、カウンタは最大値1FFFHに達するとストップしたままとなります。）

### サウンド・データの読み出し

256KビットROM IC34，IC35のメモリ・ロケーションにアクセスするには、15ビットのアドレスが必要です。残りのMSB2ビットにはIC30のA，Bクロックが当てられます。クロックCは、どちらのROMにアクセスするかを選ぶチップセレクトです。一方LSB ADR0は、音源によってはROMアドレスとして使用されません。例えば、BD−1とBD−2は同じROMのメモリ・エリアを共有しており、BD−1には偶数のアドレスがBD−2には奇数アドレスが割当てられています。（表1参照）。この為、BD−1の場合、ROMのA0には常に"0"がIC32，IC33を通じて加えられます（BD−2の場合は"1"）。

ROMから読み出されたサウンド・データは、IC37（ラダー・ネットワーク内蔵）でアナログ電圧に変換されリズム音波形の一部分（サンプリング波形）を再現しますが、振巾値は原音の値とは必ずしも一致しません。これはPCMの過程においてS/N比や分解能向上の処理が含まれている為です。再生音のエンベロープは、IC37の(+)REFに流れ込むENV GENからの信号によって左右されます。

TR-727 Sound Data ROM

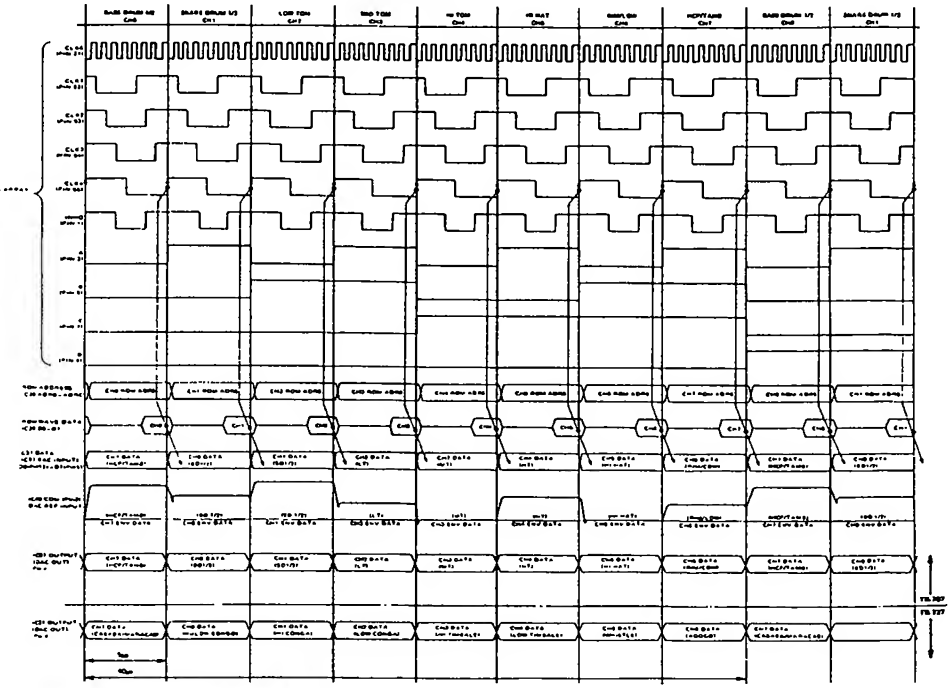
| IC NO. | ROM | CE | CS | VOICE | MEMORY |
|---|---|---|---|---|---|
| IC34 | HN61256PC71 (15179694) | H | L | HI BONGO | 2N ADRS 4k byte |
| | | | | LOW BONGO | 2N + 1 ADRS 4k byte |
| | | | | MUTE HI CONGA | 2N ADRS 4k byte |
| | | | | OPEN HI CONGA | 2N + 1 ADRS 4k byte |
| | | | | LOW CONGA | 8k byte |
| | | | | HI TIMBALE | 8k byte |
| IC35 | HN61256PC80 (15179695) | H | H | LOW TIMBALE | 8k byte |
| | | | | WHISTLE | 8k byte |
| | | | | HI AGOGO | 2N ADRS 4k byte |
| | | | | LOW AGOGO | 2N + 1 ADRS 4k byte |
| | | | | CABASA | 2N ADRS 4k byte |
| | | | | MARACAS | 2N + 1 ADRS 4k byte |

TR-707 Sound Data ROM

| IC NO. | ROM | CE | CS | VOICE | MEMORY |
|---|---|---|---|---|---|
| IC34 | HN61256PC71 (15179661) | H | L | BASS DRUM 1 | 2N ADRS 4k byte |
| | | | | BASS DRUM 2 | 2K + 1 ADRS 4k byte |
| | | | | SNARE DRUM 1 | 2N ADRS 4k byte |
| | | | | SNARE DRUM 2 | 2K + 1 ADRS 4k byte |
| | | | | LOW TOM | 8k byte |
| | | | | MID TOM | 8k byte |
| IC35 | HN61256PC72 (15179662) | H | H | HI TOM | 8k byte |
| | | | | HI HAT | 8k byte |
| | | | | RIM SHOT | 2N ADRS 4k byte |
| | | | | COW BELL | 2N + 1 ADRS 4k byte |
| | | | | HAND CLAP | 2N ADRS 4k byte |
| | | | | TAMBOURINE | 2N + 1 ADRS 4k byte |

Table 1 表1

TIMING CHART タイミング・チャート



## ENVELOPE GENERATOR

Data coming to latch IC31 is a combination of LEVEL and DYNAMICS (ACCENT). The value of LEVEL is always constant regardless of voice selected, while DYNAMICS varies with MIDI Velocity or ACCENT amount setting.

Although LEVEL/DYNAMICS is connected to all 8 ENV GENERATORs it is allowed to enter only the transistor whose base-emitter junction, for example Q26, is being forward biased by a TRIG from latch IC27 or IC28 at XSTA rate. Q26 output is then connected by IC40 to (+) REF pin of IC37 every 40μs with its level decaying according to C53xR59 time constant as the successive BD-1 data are converted to analog voltages, giving a bass drum contour to the voice.

The DAC output is boosted at Q41 and Q42 conjunction and is channeled into the S/H which is designated by A B C code placed at IC41 select pins.

As can be seen from the timing chart, the timing of enveloping and D/A converting lag one slit behind the memory addressing. That is, BD-1 sound read from ROM with channel No. ABC=000 becomes an audible sound when channel No. is represented by ABC=100. This is because the data accessed on a positive going CLK4 with ABC=000 is latched into IC36 on the next CLK4 with ABC=100. Consequently, TRIG data to ICs 27 and 28, and LEVEL/DYNAMICS data to IC31 are made to delay one CLK4 cycle to keep pace with D/A conversion at IC37

### エンベロープ，アクセント

XSTA（SXT0−7イネーブル）はIC30のアドレスカウンタに加えられると同時に、ラッチIC27，28のCKにも加えられ、BD−1が選択されている時には、ENV GENのQ26がTRIGパルスによって導通し、LEVELとDYNAMICS（ACCENT）の混合された電圧がC53に充電されます。なお、LEVELの値はどの音源の場合でも常に一定です。また、LEVEL/DYNAMICS CVは8本全てのトランジスタに印加されますが、TRIGパルスが現在加わっているトランジスタにのみに流入します。Q26の出力はIC39dを通り、IC40により時分割でD/AコンバータのREF端子へ送られて行きますが、振巾はC53×R96の時定数に応じて減衰して行きます。時定数はBDのサウンド・データ全部がROMから読み出される時間より長くなる様に設定されています。

注 IC30のアドレス・カウンタのチャンネル番号とIC40/41のチャンネル番号が異なっています。これはROMのサウンドデータが、アクセスされた時よりCLK4の1サイクル分遅れてIC36にラッチされD/A変換される為です。したがってTRIGおよびLEVEL/DYNAMICSデータもその分遅れて出力されます。

### HI HAT

Output from Q35 has no distinction between closed hi hat and open hi hat and is given a particular waveshape (decay) at VCA Q22 and IC42 as OPEN/CLOSED select signal is applied on the base of Q21.

Hi Hat に対しては、もう一度エンベロープ回路(VCA—IC42a, Q32)が追加されており、クローズかオープンかによりディケイタイムを切替えています。

### SINGLE SOUND PROCESSING

Each of CYMBAL voices (RIDE and CRASH) has dedicated sound ROM, address counter, D/A converter and envelope generator. The difference from Multiplex processing in circuit configuration is that envelope control is accomplished after the wave data becomes analog form. LEVEL/DYNAMICS (ACCENT CV) rounted to Q18 emitter (CRASH) is charged into envelope capacitor C50 on a TRIG, giving a contour to CRASH sound passing through Q14.

### シングル音源

RIDE CYMBALおよびCRASH CYMBALは、それぞれ専用のアドレス・カウンタ, ROMおよびD/Aコンバータを持っていますが動作原理はマルチ音源の場合と変りません。ただし、エンベロープがD/A変換後VCAに加えられる点が違います。

**TR-707 Sound ROM**

| IC NO. | ROM | CE | CS | VOICE | MEMORY |
|---|---|---|---|---|---|
| IC19 | HN61256PC73 (15179663) | H | L | CRASH CYMBAL | 32k byte |
| IC22 | HN61256PC74 (15179664) | H | L | RIDE CYMBAL | 32k byte |

**TR-727 Sound ROM**

| IC NO. | ROM | CE | CS | VOICE | MEMORY |
|---|---|---|---|---|---|
| IC19 | HN61256PC81 (15179696) | H | L | QUIJADA | 32k byte |
| IC22 | HN61256PC82 (15179697) | H | L | STAR CHIME | 32k byte |

Table 2 表2

# TESTING AND ADJUSTING

The built-in test program executes the following test and adjusting routines while in Test Mode.

# テストおよび調整

TR-707, TR-727 には回路機能チエックおよび調整用のプログラムが内蔵されています。このプログラムを走らせるにはテストモードに入る必要があります。

### RUNNING TEST PROGRAM

While holding down CLEAR and INSTRUMENT, switch the power ON. The unit is now in the test mode and the test program initiates test routines with TEST 1.

### テストモード

CLEARとINSTRUMENTボタンを同時に押しながら電源をオンするとテストモードとなり、テスト1が自動的に実行されます。

### TEST 1. LED SEQUENTIAL LIGHTING

Upon entering test mode the program lights up LEDs, starting with MAIN KEY 1 through SCALE INDICATOR, PATTERN GROUP and CARTRIDGE (red and green alternately) and repeats.
Leave the LEDs lighting and go to TEST 2.

### テスト1 LED順次点灯

テストモードに入ると、メインキーの1から順次LEDが点灯して行きます。CARTRIDGEのLEDは赤と緑が交互に点灯します。
LEDの点灯はくり返されますが、そのままの状態でテスト2へ進んで下さい。

### TEST 2. ALL LEDs AND LCD DOTS LIGHTING

Press ENTER and verify lighting of all LEDs and LCD dots.
Leave them lit and go to TEST 3.

### テスト2 LEDおよびLCD全点灯

ENTERを押します。全てのLEDおよびLCD上の全ドットが点灯する筈です。
そのままの状態でテスト3へ進んで下さい。

### TEST 3. SWITCHES AND ACCENT AMOUNT READING

Press ENTER. All LCD display will be cleared OFF. Referring to the illustration below, push numbered buttons 1–32 one by one and check for the lighting of corresponding dot on either Bass Drum (BonGo) or Snare Drum (Hi Conga) row on the display window.
Slide up or down ACCENT and verify that TEMPO MEASURE window reads 1 and 16 at the extremities of travel.

### テスト3 スイッチおよびアクセントレベル読込み

ENTERを押すとLCDのドットが消えます。パネル上のスイッチを押すと、右図に示す様に、対応した番号のドットがLCDの上に表示されます。

If not verified, go to ACCENT AMOUNT ADJUSTMENT below without exiting the test mode.

When all tests are satisfactory, turned the power off and on again to return to the normal operation mode (if necessary).

## ACCENT AMOUNT ADJUSTMENT

This test must be carried out in the test mode and follow the tests above.

1. Set ACCENT at MIN and adjust TM2 of VOICING board for a transition point of "1" to/from "2" of TEMPO MEASURE display reading.
2. Set ACCENT at MAX and adjust TM3 for a transition point of "15" to/from "16" of TEMPO MEASURE display reading.

The unit will remain in the test mode until the power is turned OFF.

## TEMPO CLOCK RATE ADJUSTMENT

This adjustment must be done in the normal operation mode.

1. Set TEMPO at FAST and adjust TM1 of VOICING board for 250 reading on TEMPO MEASURE window.

次に、アクセント（ＡＣ）つまみを上下させるとＬＣＤのＴＥＭＰＯ/ＭＥＡＳＵＲＥ 部に数字が表示されます。ＭＩＮの位置で"１"、ＭＡＸで"１６" とならない場合は、次のアクセントレベル調整へ進んで下さい。
調整が不要で、通常のモードに戻るには一旦電源をオフにして下さい。

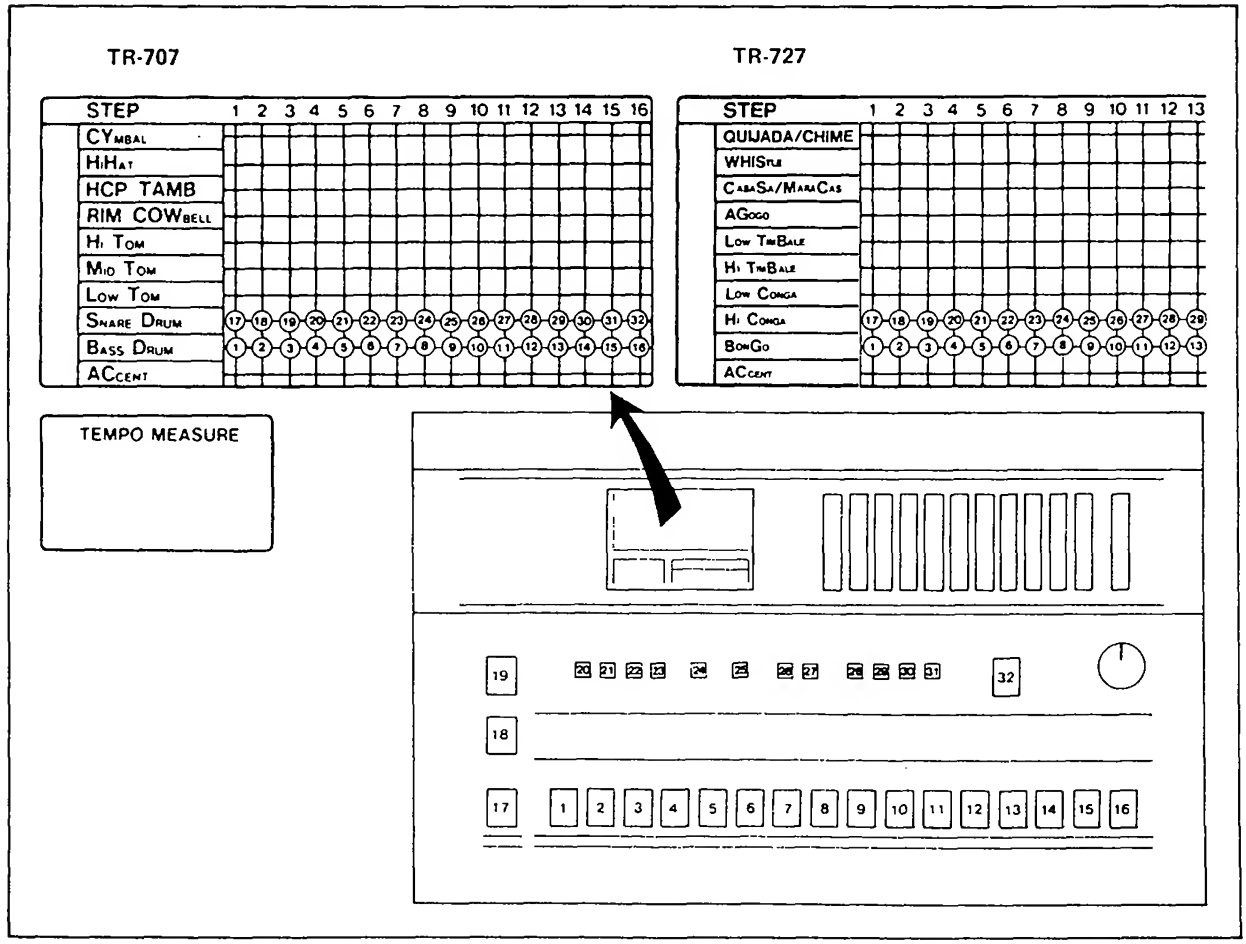
## アクセントレベル調整

本調整はテストモードで行ないます。上記のテストの後で行なって下さい。

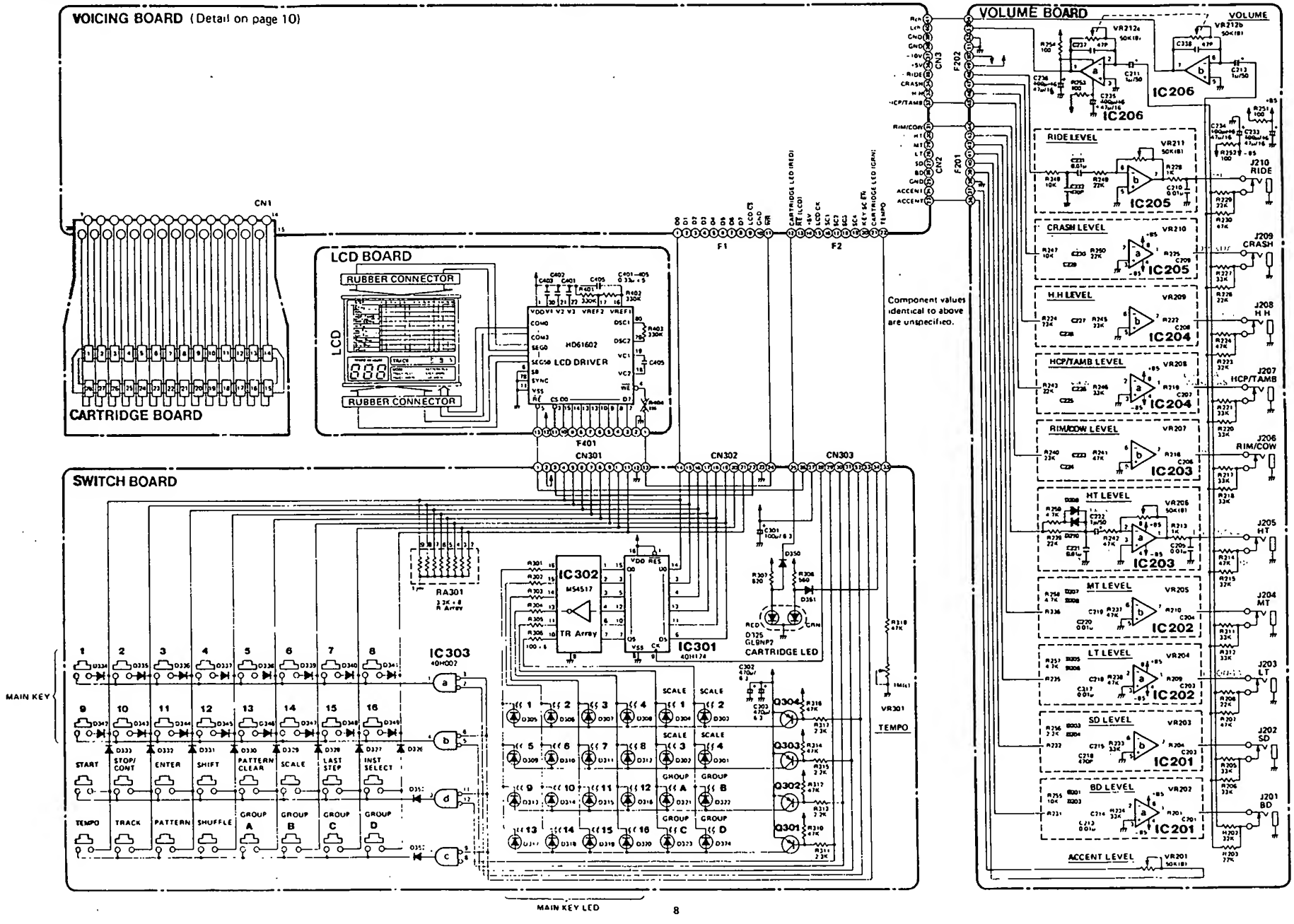
1. アクセント（ＡＣ）をＭＩＮにセットし、ＴＭ２（ボイシング基板）でＴＥＭＰＯ/ＭＥＡＳＵＲＥ の表示が"１"か"２"になる臨界点に調整します。
2. ＡＣをＭＡＸにセットし、ＴＭ３で表示が"１５"か"１６"になる臨界点に調整します。

## テンポ調整

本調整は通常のモードで行ないます。テストモードになっている場合は、一度電源をオフにして下さい。
ＴＥＭＰＯをＦＡＳＴにセットし、ＴＭＩ（ボイシング基板）でＴＥＭＰＯ/ＭＥＡＳＵＲＥの表示が２５０になる様調整します。



# TR-707/TR-727 GENERAL CIRCUIT DIAGRAM



## VOLUME BOARD

**TR-707** 7313605000 (pcb 2291098002)

**TR-727** 7313805000 (pcb 2292019000)

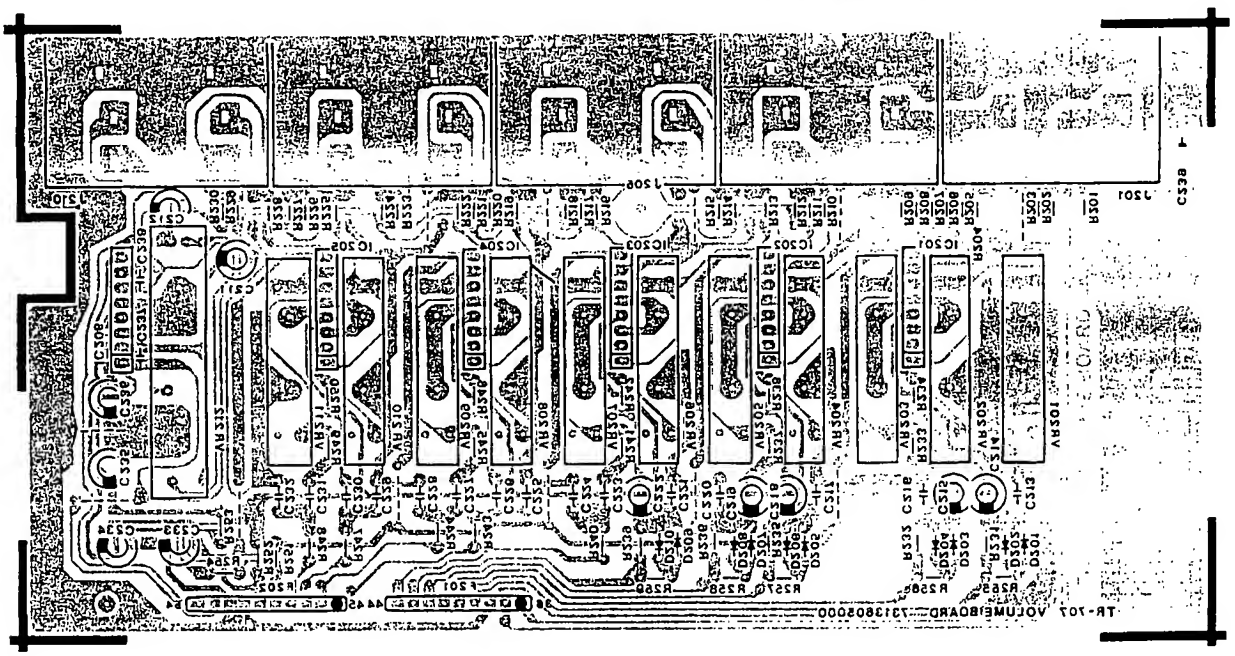
View from foil side

BELOW PCB LAYOUT For TR-707

TR-727's: identical to TR-707's except for those represented in red in the circuit diagram left.

下の基板図はTR-707用です。

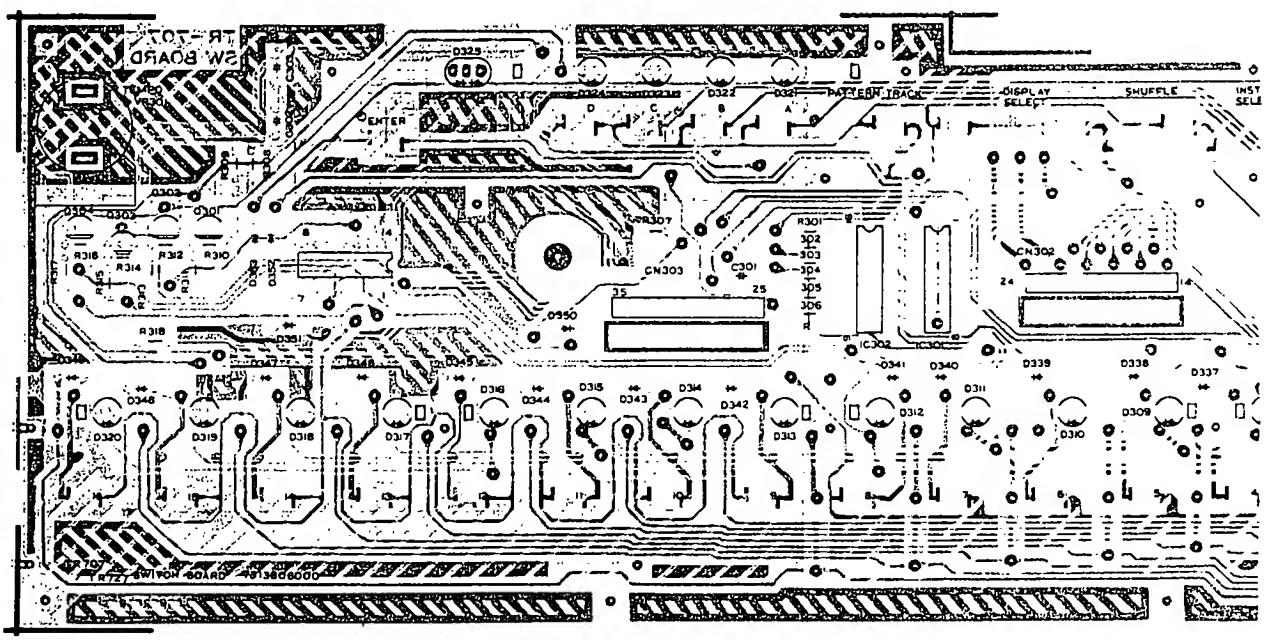
TR-727の場合は回路図の赤線表示に従って相違点を確認して下さい。



## SWITCH BOARD

7313606000 (pcb 2291097903)

View from foil side

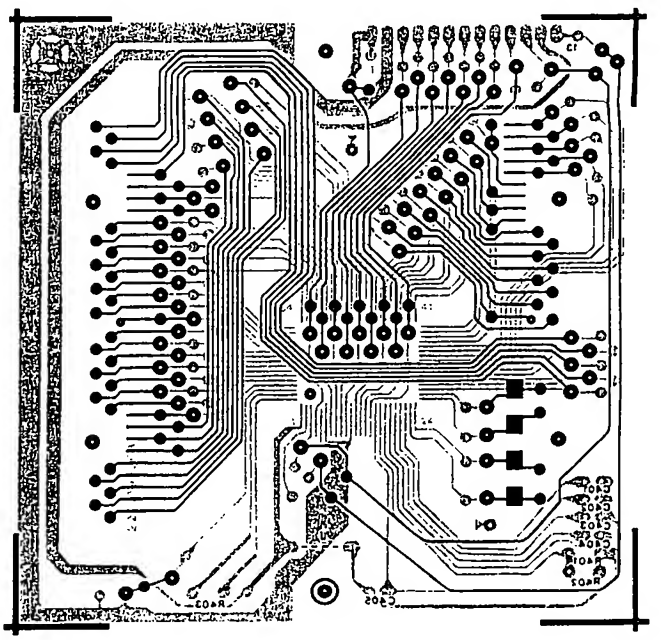


## LCD BOARD

7313607000

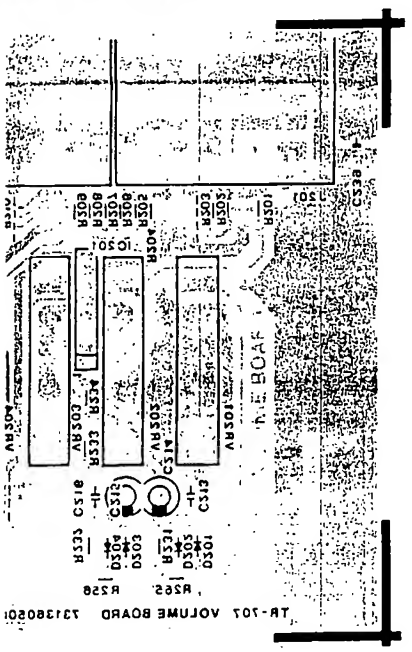
(pcb 2291098203)

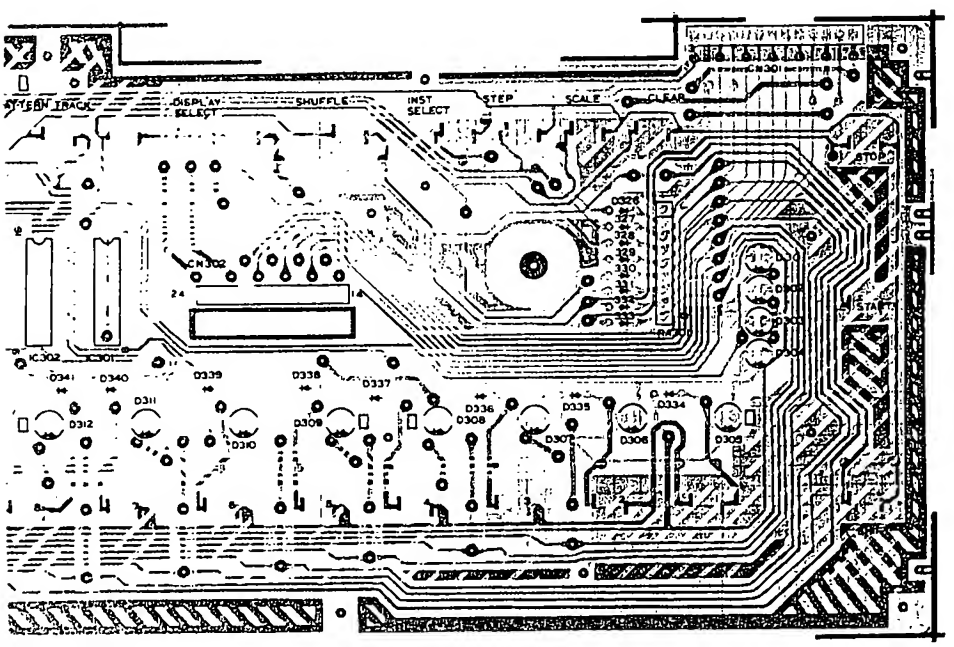
View from foil side

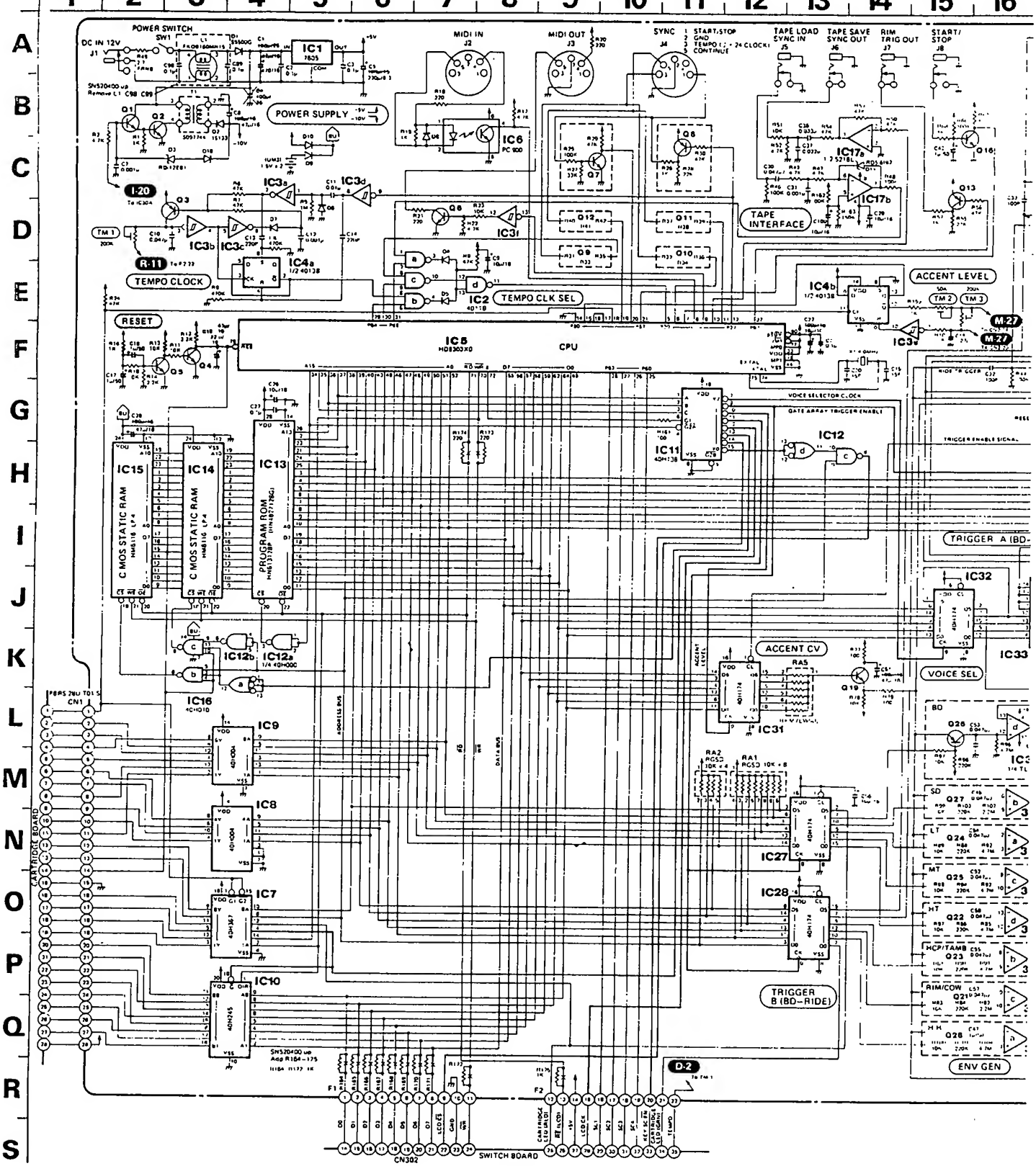


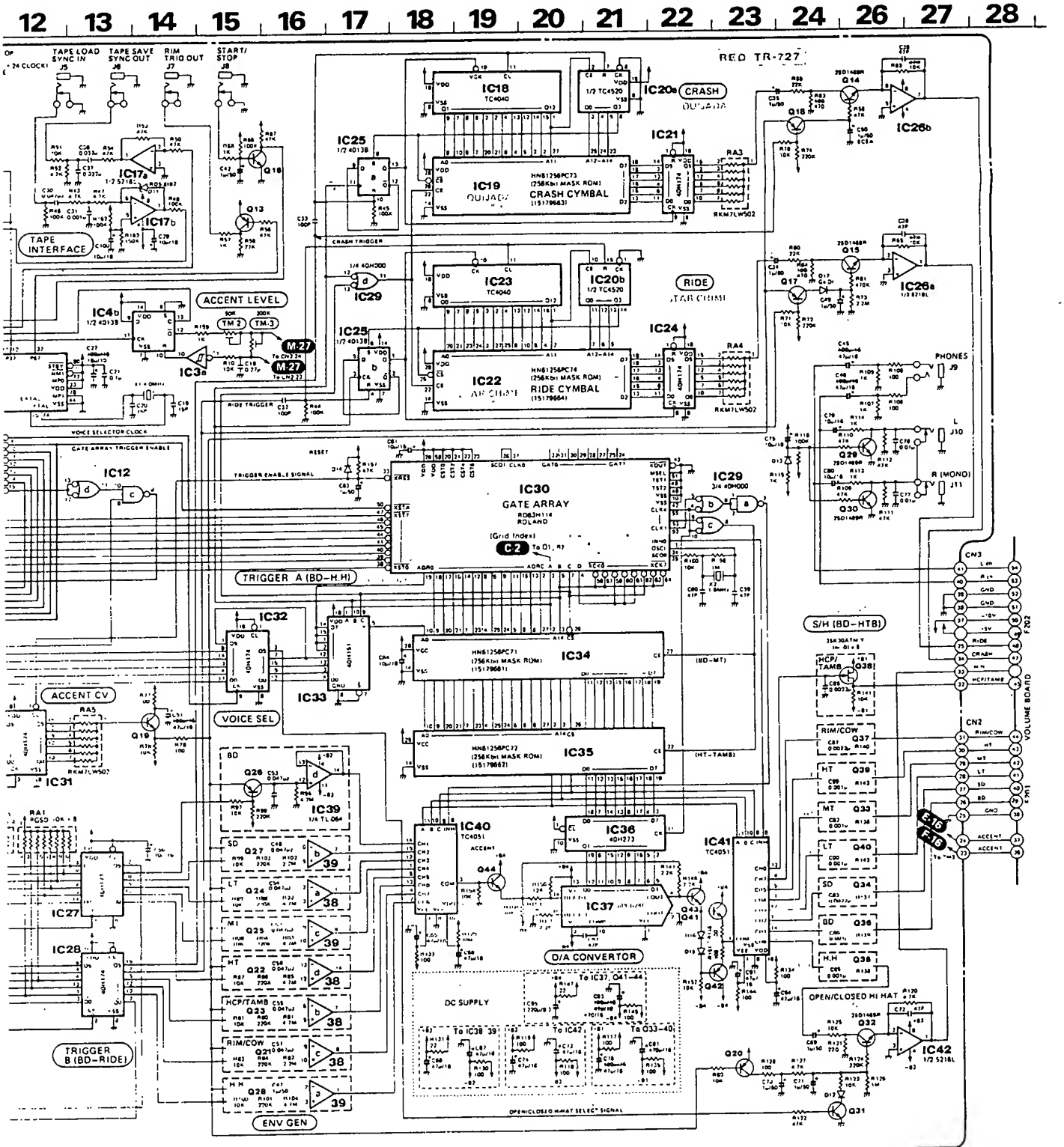
UT For TR-707

R-707's except for those represented in red
diagram left






POWER SWITCH
DC IN 12V
POWER SUPPLY
MIDI IN
MIDI OUT
SYNC
START/STOP
TAPE LOAD SYNC IN
TAPE SAVE SYNC OUT
RIM TRIG OUT
START/ STOP
TAPE INTERFACE
TEMPO CLOCK
TEMPO CLK SEL
RESET
CPU
ACCENT LEVEL
ACCENT CV
VOICE SEL
TRIGGER A (BD-
TRIGGER B (BD-RIDE)
ENV GEN
C MOS STATIC RAM
PROGRAM ROM
CARTRIDGE BOARD
SWITCH BOARD
CN302

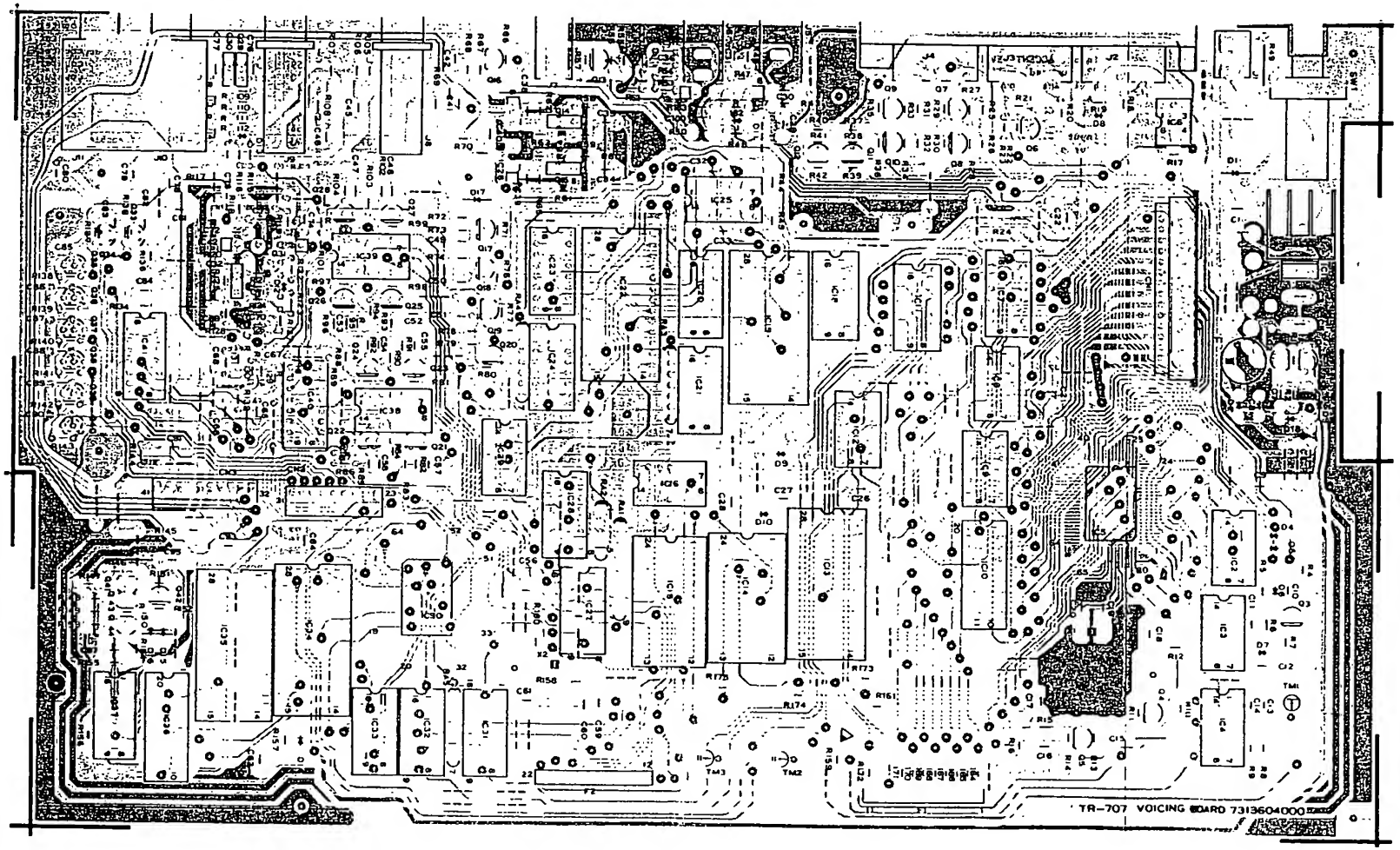

12 13 14 15 16 17 18 19 20 21 22 23 24 26 27 28
REQ TR-727
TAPE LOAD SYNC IN
TAPE SAVE SYNC OUT
RIM TRIG OUT
START/ STOP
TAPE INTERFACE
ACCENT LEVEL
IC18 TC4040
IC20a CRASH
IC19 CRASH CYMBAL
IC21
IC25
IC23 TC4040
IC20b
IC22 RIDE CYMBAL
IC24
RIDE
IC29
IC4b
IC3a
IC30 GATE ARRAY RD63H114 ROLAND
IC12
IC29
TRIGGER A (BD-H.H)
IC32
IC33
IC34
IC35
IC36 40H273
IC40 TC4051
IC41 TC4051
IC37
D/A CONVERTOR
DC SUPPLY
ACCENT CV
VOICE SEL
IC31
IC27
IC28
IC39
TRIGGER B (BD-RIDE)
ENV GEN
S/H (BD-HTB)
IC26a
IC26b
IC26c
IC42
PHONES J9
L J10
R (MONO) J11
CN3
CN2
VOLUME BOARD
OPEN/CLOSED HI HAT

# VOICING BOARD

**TR-707** 7313604000 (pcb 2291098102)
**TR-727** 7313804000 (pcb 2292018900)

BELOW PCB LAYOUT For TR-707
TR-727's: identical to TR-707's except for those represented in red in the circuit diagram left.

下の基板図はTR-707用です。
TR-727の場合は回路図の赤線表示に従って相違点を確認して下さい。

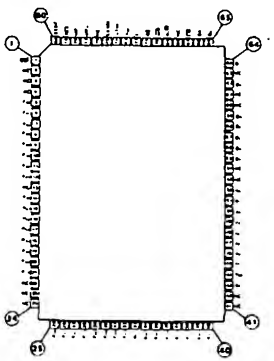



View from foil side

# IC DATA

## CPU HD6303X

Pin Configuration
(Top View)

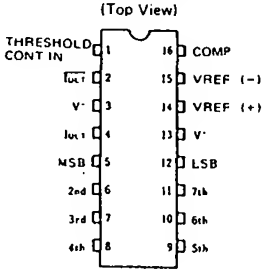


Port Assignment

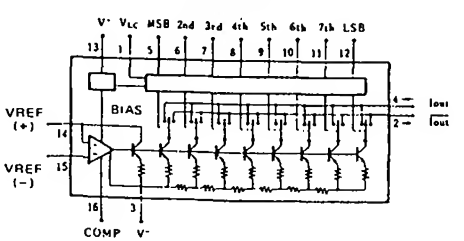
| PIN NO. | PORT NAME | DESCRIPTION |
|---|---|---|
| 1 | NMI | Unused, pulled up +5V |
| 2-4 | NC | Unused, open |
| 5 | P20 | input, TEMPO CLOCK |
| 6 | P21 | output, *TEMPO CLOCK (DIN)* |
| 7 | P22 | output, ACCENT LEVEL input trigger for internal ADC |
| 8 | P23 | input, MIDI IN |
| 9 | P24 | output, MIDI OUT |
| 10 | P25 | output, TAPE SYNC |
| 11 | P26 | output, CONT START (DIN) |
| 12 | P27 | output, START/STOP (DIN) |
| 13 | NC | unused, open |
| 14 | P50 | IRQ1 unused, pulled down |
| 15 | P51 | IRQ2<br>input, ACCENT LEVEL |
| 16 | P52 | MR unused, pulled up +5V |
| 17 | P53 | HALT unused, pulled up +5V |
| 18 | P54 | RAM cartridge control |
| 19 | P55 | input, CONT START (DIN IN) |
| 20 | P56 | input, START/STOP (DIN IN) |
| 21 | P57 | input, START/STOP from remote control |
| 22-24 | NC | unused, open |
| 25-28 | P60-P63 | output, scanning signal to LED and KEY |
| 29 | P64 | output, Internal TEMPO CLOCK |
| 30 | P65 | output, DIN SYNC TEMPO CLOCK |
| 31 | P66 | output, TAPE SYNC TEMPO CLOCK |
| 32 | P67 | output, Trigger (RIM SHOT:TR-707)(Hi AGOGO:TR-727) |
| 33 | Vcc | input, +5V power supply |
| 34-40 | A15-A9 | output, address A15---A19 |
| 41-42 | NC | unused, open |
| 43 | A8 | output, address A8 |
| 44 | Vss | GND |
| 45-52 | A7-A0 | output, address A7---A0 |
| 53-54 | NC | unused, open |
| 55-59 | D7-D3 | data bus D7---D3 |
| 60-61 | NC | unused, open |
| 62 | D2 | data bus D2 |
| 63 | NC | unused, open |
| 64-65 | D1-D0 | data bus D1---D0 |
| 66 | BA | output, unused |
| 67 | LIR | output,unused |
| 68 | NC | unused, open |
| 69 | R/W | output |
| 70 | WR | output |
| 71 | RD | output |
| 72 | E | output, system clock 1MHz |
| 73 | Vss | GND |
| 74 | XTAL | terminal, Xtal |
| 75 | EXTAL | terminal, Xtal or external system clock in |
| 76 | NC | unused, open |
| 77 | MP0 | input, MCU mode setting pulled up +5V |
| 78 | MP1 | input, MCU mode setting pulled down GND |
| 79 | RES | input, MCU reset (active low) |
| 80 | STBY | unused, pulled up +5V (active low) |

## μPC624C

Pin Configuration
(Top View)

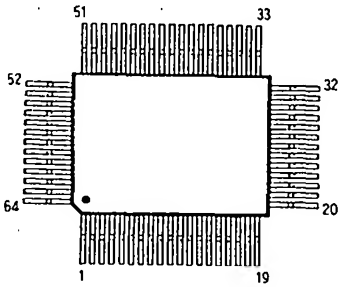



Block Diagram




## GATE ARRAY
## RD63H114

Pin Configuration
(Top View)




| Pin | name | Pin | name | Pin | name |
|---|---|---|---|---|---|
| 1 | INHO | 23 | CST6 | 45 | $\overline{XST5}$ |
| 2 | ADRC | 24 | GATE7 | 46 | $\overline{XST6}$ |
| 3 | A | 25 | GATE6 | 47 | $\overline{XST7}$ |
| 4 | D | 26 | VDD | 48 | TST1 |
| 5 | B | 27 | GATE5 | 49 | TST2 |
| 6 | ADR7 | 28 | GATE4 | 50 | XSTA |
| 7 | C | 29 | GATE3 | 51 | MSEL |
| 8 | ADR6 | 30 | GATE2 | 52 | CLK1 |
| 9 | ADR8 | 31 | GATE1 | 53 | CLK2 |
| 10 | VSS | 32 | GATE0 | 54 | CLK3 |
| 11 | ADR9 | 33 | $\overline{XRES}$ | 55 | CLK4 |
| 12 | ADR5 | 34 | OSCI | 56 | $\overline{XCK0}$ |
| 13 | ADR8 | 35 | SCO0 | 57 | $\overline{XCK1}$ |
| 14 | ADR4 | 36 | SCO1 | 58 | VDD |
| 15 | ADR3 | 37 | CLK0 | 59 | $\overline{XCK2}$ |
| 16 | ADRA | 38 | $\overline{XST0}$ | 60 | $\overline{XCK3}$ |
| 17 | ADR2 | 39 | $\overline{XST1}$ | 61 | $\overline{XCK4}$ |
| 18 | ADR1 | 40 | $\overline{XST2}$ | 62 | $\overline{XCK5}$ |
| 19 | ADR0 | 41 | $\overline{XST3}$ | 63 | $\overline{XCK6}$ |
| 20 | CST0 | 42 | VSS | 64 | $\overline{XCK7}$ |
| 21 | CST2 | 43 | $\overline{XOUT}$ | | |
| 22 | CST4 | 44 | $\overline{XST4}$ | | |

Multiple Address Counters

| DESIGNATION | PIN | DESCRIPTION | I/O |
|---|---|---|---|
| CST | 0 | pulled up (+5V) / continue start / counter 0 | I |
| | 2 | | I |
| | 4 | | I |
| | 6 | counter 6 | I |
| XST | A | XST0-XST7 enable, active low | I |
| | 0 | counter 0 | I |
| | 1 | counter 1 | I |
| | 2 | counter start, active low / counter 2 | I |
| | 3 | counter 3 | I |
| | 4 | counter 4 | I |
| | 5 | counter 5 | I |
| | 6 | counter 6 | I |
| | 7 | counter 7 | I |
| XCK | 0 | counter 0 | I |
| | 1 | counter 1 | I |
| | 2 | counter / clock input / counter 2 | I |
| | 3 | counter 3 | I |
| | 4 | counter 4 | I |
| | 5 | counter 5 | I |
| | 6 | counter 6 | I |
| | 7 | counter 7 | I |
| XOUT | | address(ADR0-ADRC) out enable, active low; high=Hi z | I |
| ADR | 0 | ROM ADDRESS | O |
| | 1 | | O |
| | 2 | | O |
| | 3 | | O |
| | 4 | | O |
| | 5 | | O |
| | 6 | | O |
| | 7 | | O |
| | 8 | | O |
| | 9 | | O |
| | A | | O |
| | B | | O |
| | C | | O |
| A | | MUX,DMUX channel select / system clock for 8 counters: 100kHz, 50kHz, 25kHz, 12.5kHz | O |
| B | | | O |
| C | | | O |
| D | | | O |
| INHO | | DMUX inhibit | O |
| OSCI | | internal clock generator | I |
| SCCO | | | O |
| SCOI | | master clock out 1.6MHz | O |
| CLK | 0 | system clock in 1.6MHz | I |
| | 1 | system clock 100kHz | O |
| | 2 | nc / latch clock — ROM chip enable — MUX inhibit | O |
| | 3 | | O |
| | 4 | | O |
| XRES | | reset pulse, active low | I |
| MSEL | | counter 12/13 bit select: pulled down | I |
| TST1 | | IC test: pulled down | I |
| TST2 | | | I |
| Vss | | GND | |
| Vss | | | |
| VDD | | power supply +5V | |
| CAT | 0 | counter gate output low=counter running | O |
| | 1 | | O |
| | 2 | | O |
| | 3 | | O |
| | 4 | | O |
| | 5 | | O |
| | 6 | | O |
| | 7 | | O |

# TR-707/TR-727 MIDI IMPLEMENTATION

## 1. TRANSMITTED DATA

| Status | Second | Third | Description |
|---|---|---|---|
| 1001 nnnn | 0kkk kkkk | 0000 0000 | Note ON *1<br>kkkkkkk = 35-51 for 5Ch, *5<br>68-74 (TR 727 only) |
| 1001 nnnn | 0kkk kkkk | 0vvv vvvv | Note ON *1<br>kkkkkkk = 35-51 for 5Ch *5<br>68-74 (TR 727 only)<br>vvvvvvv = 00 - 127 |
| 1111 0010 | 0lll llll | 0mmm mmm | Song Position Pointer *2<br>lllllll : least significant<br>mmmmmm : most significant |
| 1111 0011 | 0sss ssss | | Song Select *3<br>sssssss = 0 - 7 (track #) |
| 1111 1000 | | | Timing Clock *4 |
| 1111 1010 | | | Start |
| 1111 1011 | | | Continue |
| 1111 1100 | | | Stop |
| 1111 0000 | 0100 0001 | 0nnn nnnn | Exclusive |
| | 1111 0111 (EOX) | | Sequence Data<br>(Exclusive message) |

Notes: *1 Transmitted channel # can be changed to 1 - 16 from the front panel. When the reset is applied, the latest channel # set prior to the last power OFF remains unchanged.

*2 When any sequence number is set

*3 When the track # is set

| track # | ssssss |
|---|---|
| 1 | 0 |
| 2 | 1 |
| 3 | 2 |
| 4 | 3 |

*4

| Tempo Mode | Synchronized with |
|---|---|
| Internal | internal tempo clock |
| MIDI mode | received timing clock |
| DIN mode | positive edge of the DIN clock |

*5 Note numbers are assigned as follows.

Setting A: Normal
Setting B: When the "MIDI CH" then "LAST STEP" buttons are pressed while the "SHIFT" button is being pressed

| TR-727 Key Name | Setting A kkkkkkk | Setting B kkkkkkk |
|---|---|---|
| Hi Bongo | 60 | 35 |
| Low Bongo | 61 | 36 |
| Mute Hi Congo | 62 | 37 |
| Open Hi Congo | 63 | 38 |
| Low Congo | 64 | 39 |
| Hi Timbale | 65 | 3A |
| Low Timbale | 66 | 3B |
| Hi Agogo | 67 | 3C |
| Low Agogo | 68 | 3D |
| Cabasa | 69 | 3E |
| Maracas | 70 | 3F |
| Short Whistle | 71 | 40 |
| Long Whistle | 72 | 41 |
| Guiljada | 73 | 42 |
| Star Chime | 74 | 43 |

| TR-707 Key Name | Setting A kkkkkkk | Setting B kkkkkkk |
|---|---|---|
| Bass drum 1 | 35 | 36 |
| Bass drum 2 | 36 | 35 |
| Rim shot | 37 | 42 |
| Snare drum 1 | 38 | 38 |
| Hand clap | 39 | 45 |
| Snare drum 2 | 40 | 39 |
| Low tom | 41 | 40 |
| Closed Hi-Hat | 42 | 47 |
| Mid tom | 43 | 41 |
| Open Hi-Hat | 44 | 48 |
| High tom | 45 | 42 |
| Crash cymbal | 46 | 49 |
| Ride cymbal | 47 | 50 |
| Tambourine | 48 | 46 |
| Cowbell | 49 | 44 |

## 2. RECOGNIZED RECEIVE DATA

| Status | Second | Third | Description |
|---|---|---|---|
| 1001 nnnn | 0kkk kkkk | 0vvv vvvv | Note ON *1<br>kkkkkkk = 60-74 (TR 727) *2<br>= 35-51 for 5Ch<br>(TR-707)<br>vvvvvvv = 1 - 127 |
| 1011 0kkk | 0111 1100 | 0000 0000 | RPN, LSB |
| 1011 0kkk | 0111 1101 | 0000 0000 | RPN, MSB |
| 1111 0010 | 0lll llll | 0mmm mmm | Song Position Pointer *3<br>lllllll : least significant<br>mmmmmm : most significant |
| 1111 0011 | 0sss ssss | | Song Select *4<br>sssssss = track # |
| 1111 1000 | | | Timing Clock *5 |
| 1111 1010 | | | Start *5 |
| 1111 1011 | | | Continue *5 |
| 1111 1100 | | | Stop *5 |
| 1111 0000 | 0100 0001 | 0100 0010 | Exclusive |
| | 1111 0111 (EOX) | | Sequence Data<br>(Exclusive message) |

Notes: *1 Received channel # can be changed to 1 - 16 from the front panel. When the power is applied, the latest channel # set prior to the last power OFF remains unchanged.

*2 Recognized while in the Track Play mode
Any of the key numbers 135 - 180 may be assigned to each instrument from panel operation, and will be kept assigned even after the power is turned OFF
Received note numbers are assigned at the factory as follows

| TR-727 kkkkkkk | Instrument |
|---|---|
| 60 | Hi Bongo |
| 61 | Low Bongo |
| 62 | Mute Hi Congo |
| 63 | Open Hi Congo |
| 64 | Low Congo |
| 65 | Hi Timbale |
| 66 | Low Timbale |
| 67 | Hi Agogo |
| 68 | Low Agogo |
| 69 | Cabasa |
| 70 | Maracas |
| 71 | Short Whistle |
| 72 | Long Whistle |
| 73 | Guiriada |
| 74 | Star Chime |

| TR-707 kkkkkkk | Instrument |
|---|---|
| 35 | Bass Drum 1 |
| 36 | Bass Drum 2 |
| 37 | Rim Shot |
| 38 | Snare Drum 1 |
| 39 | Hand Clap |
| 40 | Snare Drum 2 |
| 41, *3 | Low Tom |
| *2, 46 | Closed Hi-Hat |
| 45, 47 | Mid Tom |
| 46 | Open Hi-Hat |
| 48, 50 | High Tom |
| 49 | Crash Cymbal |
| 51 | Ride Cymbal |
| 54 | Tambourine |
| 56 | Cowbell |

All the note OFF messages are ignored

*3 Recognized while the unit STOPS in the Track Play mode
*4 When the SYNC mode is at MIDI

While in the Tape Interface mode, all MIDI messages are rejected

## 3. HANDSHAKING COMMUNICATION

### 3.1 Message Type

3.1.1 Want to send a file (WSF)

| Byte | Description |
|---|---|
| a 1111 0000 | Exclusive status |
| b 0100 0001 | Roland ID # |
| c 0101 0000 | Operation code |
| d 1111 0111 | End of System Exclusive |

3.1.2 Request a file (RQF)

| Byte | Description |
|---|---|
| a 1111 0000 | Exclusive status |
| b 0100 0001 | Roland ID # |
| c 0101 0001 | Operation code |
| d 1111 0111 | End of System Exclusive |

3.1.3 Data (DAT)

| Byte | Description |
|---|---|
| a 1111 0000 | exclusive status |
| b 0100 0001 | Roland ID # |
| c 0101 0010 | Operation code |
| d 0000 0010 | Format type |
| e 0100 nnnn | Block # (0 - 127) |
| f 0000 xxxx | |
| 0000 yyyy | 512 data bytes (256 bytes of assessment) |
| 0000 xxxx | |
| 0000 yyyy | |
| g 0sss ssss | Check sum (for preceding 512 data bytes) |
| h 1111 0111 | End of System Exclusive |

Note:
Summed value of the all bytes in data and the check sum must be 0 (7 bits)

3.1.4 Acknowledge (PAS)

| Byte | Description |
|---|---|
| a 1111 0000 | Exclusive status |
| b 0100 0001 | Roland ID # |
| c 0101 0011 | Operation code |
| d 1111 0111 | End of System Exclusive |

3.1.5 Continue (CNT)

| Byte | Description |
|---|---|
| a 1111 0000 | Exclusive status |
| b 0100 0001 | Roland ID # |
| c 0101 0100 | Operation code |
| d 1111 0111 | End of System Exclusive |

3.1.6 End of File (EOF)

| Byte | Description |
|---|---|
| a 1111 0000 | Exclusive status |
| b 0100 0001 | Roland ID # |
| c 0101 0101 | Operation code |
| d 1111 0111 | End of System Exclusive |

3.1.7 Communication error (ERR)

| Byte | Description |
|---|---|
| a 1111 0000 | Exclusive status |
| b 0100 0001 | Roland ID # |
| c 0111 0001 | Operation code |
| d 1111 0111 | End of System Exclusive |

3.1.8 Rejection (RJC)

| Byte | Description |
|---|---|
| a 1111 0000 | Exclusive status |
| b 0100 0001 | Roland ID # |
| c 0111 0010 | Operation code |
| d 1111 0111 | End of System Exclusive |

### 3.2 Sequence of Communication

3.2.1 When the RQF is recognized

| | | |
|---|---|---|
| a RQF | Request a File | (received) |
| b DAT | Data | (transmitted) |
| CNT | Continue | (transmitted) |
| PAS | Acknowledge | (received) |
| | (Six times) | |
| c DAT | Data | (transmitted) |
| EOF | End of File | (transmitted) |
| PAS | Acknowledge | (received) |

3.2.2 When the WSF is recognized

| | | |
|---|---|---|
| a WSF | Want to Send a File | (received) |
| b RQF | Request a File | (transmitted) |
| c DAT | Data | (received) |
| CNT | Continue | (transmitted) |
| PAS | Acknowledge | (transmitted) |
| | (Six times) | |
| d DAT | Data | (received) |
| EOF | End of File | (received) |
| PAS | Acknowledge | (transmitted) |

3.2.3 When the WSF is received with error

| | | |
|---|---|---|
| a WSF | Want to Send a File | (received) |
| b RJC | Rejection | (transmitted) |
| | (The sequence will abort then return to normal operation.) | |

3.2.4 When the RQF is received with error

| | | |
|---|---|---|
| a RQF | Request a File | (received) |
| b RJC | Rejection | (transmitted) |
| | (The sequence will abort then return to normal operation.) | |

3.2.5 When the ERR is recognized

| | | |
|---|---|---|
| DAT | Data | (transmitted) |
| CNT | Continue | (transmitted) |
| ERR | Communication error | (received) |
| DAT | Data (same block) | (transmitted) |
| CNT | Continue | (transmitted) |

3.2.6 When DAT or others is received with errors

| | | |
|---|---|---|
| DAT | Data | (received) |
| ERR | Communication error | (transmitted) |

The unit will expect to receive the previous DAT